UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,643	07/07/2006	**Takanori Okada**	056937-0295	5463

53080 7590 12/10/2008

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER	
GIARDINO JR, MARK A	
ART UNIT	PAPER NUMBER
2185	
MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,643	OKADA ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 9/9/2008. At this point claims 1-18 have been amended and no claims have been added or cancelled . Thus, claims 1-18 are pending in the instant application.

The instant application having Application No. 10/585,643 has a total of 18 claims pending in the application, there are 18 independent claims and no dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-10, and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by **Chiba (US 6,401,166).**

Regarding Claim 1, Chiba teaches a non-volatile semiconductor recording medium (flash memory 1 of Figure 1) comprising:

A plurality of erasing blocks, each erasing block being a first size and physically erasable as a single unit (Chiba teaches the flash is erasable by blocks, where each block is erasable as a single unit, Column 1 Lines 21-24);

a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26);

and a partition region (data region beginning with Cluster 4 of Figure 4), wherein

an information on a start position of the partition region is recorded in the partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26),

the start position information includes a value at which a predetermined region is secured between a terminal end of the partition management information region and a starting end of the partition region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 27-32), and

the region secured between the terminal end of the partition management information region and the starting end of the partition region is larger than the first size and is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25, also since the partition region begins at Cluster 4, the region between the terminal end of the partition

management information region and the starting end of the partition region contains two blocks [Cluster 2 and Cluster 3] and thus is larger than an erasable block).

Regarding Claim 2, Chiba teaches a non-volatile semiconductor recording medium (flash memory 1 of Figure 1) comprising:

a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26);

a first partition region (Clusters 2 and 3 data regions of Figure 4); and

a second partition region located after the first partition region (Clusters 6 and 7 of Figure 4); wherein

a single address space includes a first address value corresponding to the beginning of the first partition region, a second address value corresponding to the terminal end of the first partition region, and a third address value corresponding to the beginning of the second partition region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 27-32);

the first and third address values are recorded in the partition management information region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 27-32);

the second and third address values are not consecutive, and are separated by at least three consecutive address values corresponding to a switch region located between the first and second partition regions (Figure 4 clearly shows the separation between the second and third address values, and Blocks 4 and 5 corresponds to the switch region and is between the first and second partition regions); and

the switch region is physically erased (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block").

Regarding Claim 3, Chiba teaches a non-volatile semiconductor recording medium (flash memory 1 of Figure 1) comprising:

a plurality of erasing blocks, each erasing block being a first size and physically erasable as a single unit (Chiba teaches the flash is erasable by blocks, where each block is erasable as a single unit, Column 1 Lines 21-24); wherein

information is recorded according to a recording format of a predetermined file system (FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64),

a region which is not used for the recording is larger than the first size and is included in the recording format of the file system (FAT/Directory Regions of Figure 16, the directory region is used for overhead and not recorded, Column 2 Lines 52-56),

and the region which is not used for the recording is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the boot region is created while the other regions remain in a state

where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25, also the FAT/Directory region in Figure 16 is clearly larger than the erasable block size, and Figure 18 clearly shows how the steps of Figure 4 are used in this embodiment).

Regarding Claim 6, Chiba teaches a non-volatile semiconductor recording medium of non-volatile semiconductor (flash memory 1 of Figure 1) in which information is recorded according to a recording format of FAT file system (Chiba uses the FAT file system, which uses "a table indicating an allocation of the file", Column 8 Line 64),

wherein a user data region comprising a plurality of clusters (data regions of Figure 4, which also shows a plurality of clusters among the data regions) and a file allocation table region (FAT region of Figure 4) are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region (since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT records information on the state of the clusters, Column 14 Lines 3-4);

the file allocation table region indicates that a continuous series of at least three clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster (the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region would indicate that a continuous series of at least three clusters are used),

and a region of the user data region corresponding continuous series of at least three clusters is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25).

Claim 7 is the method equivalent to Claim 1, and is rejected under similar rationale.

Claim 8 is the method equivalent of Claim 2, and is rejected under similar rationale.

Claim 9 is the method equivalent to Claim 3, and is rejected under similar rationale.

Claim 12 is the method equivalent to Claim 6, and is rejected under similar rationale.

Claim 13 is the information recording format equivalent to Claim 1, and is rejected under similar rationale.

Claim 14 is the information recording format equivalent to Claim 2, and is rejected under similar rationale.

Claim 15 is the information recording format equivalent to Claim 3, and is rejected under similar rationale.

Claim 18 is the information recording format equivalent to Claim 6, and is rejected under similar rationale.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 10, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Murray et al (US 6,185,666).

Regarding Claim 4, Chiba teaches a non-volatile semiconductor recording medium (flash memory 1 of Figure 1) comprising:

a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26);

and a partition containing a FAT file system (the entire flash memory that does not contain the master boot memory region of Figure 4); wherein

an information on a start position of the partition is recorded in the partition management information region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 27-32);

the partition comprises a partition boot information region and a file allocation

table region (partition boot memory region of Figure 4 and File Allocation Table of Figure 4), and

the regions in a state where data is physically erased (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block").

However, Chiba does not teach reserved sectors between the two partitions. Murray teaches a plural number of reserved sectors, the reserved sectors being positioned in the partition between the partition boot information region and a starting end of the file allocation table region (Figure 4 of Murray).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have included a reserved section as in Murray in the flash device of Chiba because the reserved area can contain important information about the function of the memory device (Column 7 Lines 21-29), thus allowing the memory to operate better.

Claim 10 is the method equivalent to Claim 4, and is rejected under similar rationale.

Claim 16 is the information recording format equivalent to Claim 4, and is rejected under similar rationale.

Claims 5, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba in view of Nakamura et al (US 6,873,789) and Murray.

Regarding Claim 5, Chiba teaches a non-volatile semiconductor recording

medium (flash memory 1 of Figure 1) comprising:

a partition management information region (master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26);

a partition containing a file system (the entire flash memory that does not contain the master boot memory region of Figure 4), wherein

an information on a start position of the partition is recorded in the partition management information region (the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition begins and ends, Column 8 Lines 27-32),

the partition comprises a partition descriptor information region and a space bit map region (the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32);

an information on a start position of the space bit map region is recorded in the partition descriptor information region (the “partition boot memory region stores information about a structure of each partition”, Column 8 Lines 39-42), and

the region secured prior to the starting end of the space bit map region is in a state where data is physically erased (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”).

However, Chiba does not teach a region of a plurality of memory blocks secured prior to a starting end of the space bit map region. Murray teaches a plural number of

reserved [secured] sectors, the reserved sectors being positioned in the partition between the partition boot information region and a starting end of the file system region (Figure 4 of Murray).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have included a reserved section as in Murray in the flash device of Chiba because the reserved area can contain important information about the function of the memory device (Column 7 Lines 21-29), thus allowing the memory to operate better.

Further, Chiba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system (Column 6 Lines 22-25) with a space bit map in memory (Column 12 Lines 52-53). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chiba and to use a UDF file system in place of the FAT file system, so that the memory device of Chiba can be compatible with operating systems that use the UDF file system.

Claim 11 is the method equivalent to Claim 5, and is rejected under similar rationale.

Claim 17 is the information recording format equivalent to Claim 5, and is rejected under similar rationale.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 1, 3, 7, 9, 13, and 15 have been considered but are not persuasive. While the empty region of Chiba may be less than an erasable block, if the partition region is defined as the region that begins with Cluster 4 of Figure 4, the region between the terminal end of the partition management information region and the starting end of the partition region is larger than the erasable block size and is in a state where data is physically erased. Additionally, the embodiment of Figure 16 reads on some of the claims as described in the action above.

Applicant's argument regarding Claim 1, 6, 12, and 18 that the erasing of Chiba would take a great deal of time has been considered but is not persuasive. The length of time regarding the erasing process is not mentioned in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's argument regarding Claim 15 has been considered and has been changed in the action; Claim 15 is the information recording equivalent to Claim 3 and Claim 14 is the information recording equivalent to Claim 2.

Applicant's arguments regarding Claims 2, 8, and 14 have been considered but are moot in view of the new grounds of rejection.

Applicant's arguments regarding Claims 4, 10, and 16 have been considered but are moot in view of the new grounds of rejection.

Applicant's arguments regarding Claims 5, 11, and 17 have been considered but are moot in view of the new grounds of rejection.

Applicant's arguments regarding Claim 6, 12, and 18 have been considered but are not persuasive. Chiba teaches three continuous series of clusters that are continually erased as described in the office action above.

CLOSING COMMENTS

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a second action on the merits and are subject of a second action final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino /Sanjiv Shah/

/M.G./

Supervisory Patent Examiner, Art Unit 2185

Patent Examiner
Art Unit 2185

December 9, 2008